A Pulse-Frequency-Modulated Full-Bridge DC/DC Converter With Series Boost Capacitor

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Abstract—The conventional zero-voltage switching phase-shift full-bridge (ZVS PSFB) converter has a large circulating energy during the freewheeling interval caused by the small duty cycle, which could increase the primary-side conduction losses, the turn-off switching losses of lagging-leg switches, and the current ripple through the output inductor. To overcome these problems, this paper proposes a new pulse-frequency-modulated full-bridge direct-current (dc)/dc converter with a series boost capacitor (SBC). The proposed converter controls the output voltage by varying the voltage across the SBC according to the switching frequency and has no freewheeling interval due to a 50% fixed duty operation. As a result, since its freewheeling current is eliminated, the conduction losses can be considerably reduced, as compared with those of the conventional ZVS PSFB converter. Moreover, the ZVS of all power switches cannot only be ensured along wide load ranges, but the current ripple through the output inductor can be also significantly reduced. Therefore, it has very desirable merits such as high efficiency, small output inductor, and improved heat generation. Operational principles, theoretical analysis, and design considerations are presented. To confirm the operation, the validity, and the features of the proposed converter, experimental results from a prototype that is 400–12 V/100 A are presented.

Index Terms—Full bridge, pulse-frequency modulation (PFM), series boost capacitor (SBC).

I. INTRODUCTION

RECENTLY, many direct-current (dc)/dc topologies for the distributed power supply of telecommunication or server systems have been developed, which characterize the high efficiency and the high power density. Among these topologies, a conventional zero-voltage switching phase-shift full-bridge (ZVS PSFB) converter has received considerable attentions for medium- or high-power applications, which is because it features high conversion efficiency, high power density, and low electromagnetic interference (EMI). Many literatures have already analyzed its operation principles and design considerations in detail [1]–[4].

Since the holdup time requirement, which is defined as the time duration that a power supply should remain its output voltage regulated even at an instant power failure of utility, must be considered for the power supply of telecommunication or server systems, the ZVS PSFB converter should be fit for a relatively wide input voltage range. Thus, the steady-state duty cycle is as small as approximately 30% at a normal operating condition, as shown in Fig. 1(c).

This small duty cycle has detrimental effects on the converter performance, such as an increased circulating current and associated conduction loss, and a large ripple current through the output inductor $L_o$. Moreover, since the energy stored in the small leakage inductor is not large enough to achieve the ZVS of lagging-leg switches under light load conditions, hard switching operation and poor EMI performance are inevitable [5]. To cope with these problems, zero-voltage and zero-current switching techniques, which can reduce the turn-on and turn-off switching losses and circulating energy during the freewheeling interval, are preferred in these kinds of applications [6]–[19]. However, all these approaches have the common practical drawbacks such as narrow ZVS ranges, circulating current, large output ripple current, and limited efficiency originated from the small duty cycle at the steady state.

In this paper, a full-bridge dc/dc converter using a series boost capacitor (SBC) controlled by pulse-frequency modulation (PFM) is proposed, as shown in Fig. 2. The proposed converter has a similar circuit configuration to the conventional series resonant converter (SRC). However, it uses a resonance between the magnetizing inductance $L_m$ and the
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Fig. 1. Conventional ZVS PSFB converter. (a) Circuit configuration; (b) key waveforms; and (c) the voltage conversion ratio $M$ and current ripple ratio $r$ of the output inductor.

Fig. 2. Schematic of the proposed PFM-SBC full-bridge dc/dc converter.

resonant capacitor $C_r$, whereas the SRC employs a resonance between the leakage inductance $L_k$ and the resonant capacitor $C_r$. Moreover, the switching frequency of the proposed converter is not varied too much along a wide load range, whereas that of the SRC is widely varied. In particular, since the SRC has no output filter inductor, it has several drawbacks such as large current stress of each device, large root-mean-square (RMS) current, and subsequent poor conduction losses.

The proposed converter controls the output voltage by varying the voltage across the SBC according to the switching frequency and has no freewheeling interval with the aid of a 50% fixed duty operation. Therefore, its conduction loss is lower than that of the conventional ZVS PSFB converter. Moreover, the ZVS operation of all power switches can be achieved under wide load ranges, and the operating frequency can have small variation from no load to full load. The current ripple of the output inductor is very small; thus, the output inductor can be smaller than that of the ZVS PSFB converter ($L_o$, $\alpha < 1$) and can be more reduced than that of the ZVS PSFB converter ($L_o$). These advantages make the proposed converter well suited for high-power and high-current applications such as the power supply for telecommunication or server systems.

The operations, the analysis, the design considerations, and the experimental results are presented to confirm the validity of the proposed converter.

Fig. 3. Voltage waveform on the rectified voltage $V_{\text{rec}}$ according to the switching frequency.

II. OPERATIONAL PRINCIPLES

A. Operation Principles

Fig. 2 shows the proposed PFM-SBC full-bridge converter. The gate signals of $M_1$ (and $M_2$) and $M_3$ (and $M_4$) are complementarily conducted with small dead times in order to avoid shoot-through. Fig. 3 shows $v_{\text{rec}}$ according to the switching frequency, where $v_{\text{rec}}$ is the rectified voltage on the secondary side. As shown in this figure, areas A and B are the negative and positive portions of $[v_{\text{rec}}(t) - V_{\text{in}}/n]$, respectively. In addition, $v_{\text{rec}}(t)$ can be expressed as $v_{\text{rec}}(t) = \{V_{\text{in}} - v_{C_r}(t)\}/n$. Assuming that the input voltage $V_{\text{in}}$ is constant, the waveform of $v_{\text{rec}}(t)$ is varied by the voltage of the boost capacitor $v_{C_r}(t)$, and the output voltage $V_o$ is obtained by smoothing $v_{\text{rec}}(t)$ by the output $L-C$ filter. Therefore, the average value of $v_{\text{rec}}(t)$ is equal to the output voltage $V_o$. Since the voltage across the boost capacitor $v_{C_r}(t)$ is determined by the switching frequency, the proposed converter adjusts the switching frequency of $M_1-M_4$ in order to regulate the output voltage. Since the difference between areas A and B is large at low frequencies, the output voltage is higher than $V_{\text{in}}/n$. On the other hand, since the difference between areas A and B is small at high frequencies, the output voltage approaches $V_{\text{in}}/n$. Through the aforementioned mechanism, the output voltage can be regulated by the PFM.
as follows.

For the convenience of the converter. One switching period is divided into two modes, B. Mode Analysis

Fig. 4 shows the operational key waveforms of the proposed converter.

Fig. 4. Operational key waveforms of the proposed converter.

**B. Mode Analysis**

Fig. 4 shows the operational key waveforms of the proposed converter. One switching period is divided into two modes, and each equivalent circuit is shown in Fig. 5. The gates of $M_1$ (and $M_2$) and $M_3$ (and $M_4$) are complementarily turned on and off with a 50% fixed duty. For the convenience of the mode analysis in the steady state, several assumptions are made as follows.

1) All parasitic components except those specified in Fig. 3 are neglected.
2) The transformer leakage $L_k$ is small enough to be ignored.
3) Current $I_{Lo}$ through the output inductor $L_o$ is constantly equal to $I_o$.
4) There is no dc offset current of the transformer magnetizing inductor $L_m$.
5) The dead time between switches $M_1$, $M_2$, and $M_3$, $M_4$ is small enough to be ignored.

Before $t_0$, it is assumed that $M_3$ and $M_4$ are conducting and the input power is transferred to the output side by $M_3$, $M_4$, the transformer, and $D_{S2}$.

**Mode 1 ($t_0$–$t_1$):** When $M_1$ and $M_2$ are turned on at $t_0$, mode 1 begins, as shown in Fig. 5(a). The input power is transferred to the output side by $M_1$, $M_2$, the transformer, and $D_{S1}$. Since $D_{S1}$ is conducting during $t_0$–$t_1$, $I_o$ is reflected to the transformer primary side, and $-V_{in} - v_{Cr}(t)$ is applied to the magnetizing inductor $L_m$. Therefore, $i_{lm}(t)$ and $i_{pri}(t)$ are expressed as follows:

$$i_{lm}(t) = i_{lm}(t_0) + \left(\frac{V_{in} - v_{Cr}(t)}{L_m}\right)(t - t_0) \quad (3)$$

$$i_{pri}(t) = i_{lm}(t) + \frac{I_o}{n}. \quad (4)$$

The voltage across the boost capacitor $v_{Cr}(t)$ is charged by $i_{pri}(t)$ as follows:

$$v_{Cr}(t) = V_{Cr}(t_0) + \int_{t_0}^{t} i_{pri}(t)dt$$

$$= V_{Cr}(t_0) + \int_{t_0}^{t} \left( i_{lm}(t_0) + \left(\frac{V_{in} - v_{Cr}(t)}{L_m}\right) \times (t - t_0) + \frac{I_o}{n} \right)dt. \quad (5)$$

**Mode 2 ($t_1$–$t_2$):** After $M_1$ and $M_2$ are turned off at $t_1$, the input power is transferred to the output side by $M_3$, $M_4$, the transformer, and $D_{S2}$, as shown in Fig. 5(b). Since $D_{S2}$ is conducting during $t_1$–$t_2$, $I_o$ is reflected to the transformer primary side, and $-V_{in} - v_{Cr}(t)$ is applied to the magnetizing inductor $L_m$. Therefore, $i_{lm}(t)$ and $i_{pri}(t)$ are expressed as follows:

$$i_{lm}(t) = i_{lm}(t_1) - \left(\frac{V_{in} + v_{Cr}(t)}{L_m}\right)(t - t_1) \quad (6)$$

$$i_{pri}(t) = i_{lm}(t) - \frac{I_o}{n}. \quad (7)$$

The voltage across the boost capacitor $v_{Cr}(t)$ is discharged by $i_{pri}(t)$ as follows:

$$v_{Cr}(t) = V_{Cr}(t_1) + \int_{t_1}^{t} i_{pri}(t)dt$$

$$= V_{Cr}(t_1) + \int_{t_1}^{t} \left( i_{lm}(t_1) - \left(\frac{V_{in} + v_{Cr}(t)}{L_m}\right) \times (t - t_1) - \frac{I_o}{n} \right)dt. \quad (8)$$

When $M_3$ and $M_4$ are turned off, this mode 2 ends at $t_2$. Subsequently, the operation from $t_0$ to $t_2$ is repeated.

**III. ANALYSIS OF THE PROPOSED CONVERTER**

A. Voltage Conversion Ratio

To simplify the analysis of the voltage conversion ratio, the leakage inductance $L_K$ and the dead time between switches $M_1$ (and $M_2$) and $M_3$ (and $M_4$) are neglected.

Fig. 6 is an equivalent circuit diagram that operates during $t_0$–$t_1$. As shown in this figure, a resonant $L_C$ circuit is formed, and $v_{Cr}(t)$ and $i_{lm}(t)$ are expressed as follows:

$$C \frac{dv_{Cr}(t)}{dt} = i_{lm}(t) + \frac{I_o}{n} \quad (9)$$

$$V_{in} = v_{Cr}(t) + L_m \frac{di_{lm}(t)}{dt} \quad (10)$$

where $C_r$ and $L_m$ have the following initial values:

$$v_{Cr}(t_0) = -V_r \quad i_{lm}(t_0) = -I_r. \quad (11)$$
Fig. 5. Equivalent circuits of the proposed converter. (a) Mode 1 ($t_0 \to t_1$). (b) Mode 2 ($t_1 \to t_2$).

Therefore, $v_{Cr}(t)$ and $i_{Lm}(t)$ can be derived from (9) and (11) as

$$v_{Cr}(t) = -Z \left( I_V - \frac{I_o}{n} \right) \sin(\omega_o t) - (V_V + V_{in}) \cos(\omega_o t) + V_{in}$$

$$i_{Lm}(t) = -\left( I_V - \frac{I_o}{n} \right) \cos(\omega_o t) + \frac{(V_V + V_{in})}{Z} \sin(\omega_o t) - \frac{I_o}{n}$$

where the characteristic impedance $Z$ and the resonant angular frequency $\omega_o$ are defined as

$$Z = \sqrt{\frac{L_m}{C_r}}$$
$$\omega_o = \frac{1}{\sqrt{L_mC_r}}.$$

Since $v_{Cr}(t)$ and $i_{Lm}(t)$ become $V_V$ and $I_V$ after a half switching cycle, respectively, the following equations are satisfied:

$$V_V = -Z \left( I_V - \frac{I_o}{n} \right) \sin \left( \omega_o \frac{T_s}{2} \right)$$

$$- (V_V + V_{in}) \cos \left( \omega_o \frac{T_s}{2} \right) + V_{in}$$

$$I_V = -\left( I_V - \frac{I_o}{n} \right) \cos \left( \omega_o \frac{T_s}{2} \right)$$

$$+ \frac{(V_V + V_{in})}{Z} \sin \left( \omega_o \frac{T_s}{2} \right) - \frac{I_o}{n}.$$

From (11), (15), and (16), $V_V$ and $I_V$ can be derived from (11) as

$$V_V = Z \frac{I_o}{n} \frac{\sin(0.5\omega_o f_{sw})}{1 + \cos(0.5\omega_o f_{sw})}$$

$$I_V = V_{in} \frac{\sin(0.5\omega_o f_{sw})}{Z} \frac{1 + \cos(0.5\omega_o f_{sw})}{1 + \cos(0.5\omega_o f_{sw})}.$$

As shown in Fig. 3, since the average of $v_{rec}(t)$ is equal to the output voltage $V_o$, $V_o$ can be expressed as

$$V_o = \frac{1}{T_s/2} \int_0^{T_s/2} \left[ \frac{1}{n} \{V_{in} - V_{Cr}(t)\} \right] dt$$

$$= \frac{2}{nT_s} \left[ \frac{Z}{\omega_o} \left( I_V - \frac{I_o}{n} \right) \left\{ \cos \left( \omega_o \frac{T_s}{2} \right) - 1 \right\} \right.$$

$$- \frac{V_V + V_{in}}{\omega} \sin \left( \omega_o \frac{T_s}{2} \right) \left\} \right].$$

Therefore, the voltage conversion ratio of the proposed converter can be derived from (17)–(19) as

$$\frac{nV_o}{V_{in}} = \frac{2}{\pi(f_o/f_{sw})} \frac{\sin(\pi f_o f_{sw})}{1 + \cos(\pi f_o f_{sw})}.$$

where $f_o$ and $f_{sw}$ are the resonant frequency $1/2\pi(L_mC_r)^{0.5}$ and the switching frequency, respectively. From (20), the voltage conversion ratio is dependent on $f_{sw}$, $f_o$, and $n$. Based on (20), Fig. 7 shows the theoretical voltage conversion ratio according to the normalized switching frequency by the resonant frequency.

B. ZVS

Since the switching operations of $M_1$ (and $M_2$) and $M_3$ (and $M_4$) are symmetrical, only $M_1$ is considered. The ZVS of switch $M_1$ is achieved by the energy stored in the leakage inductor. Therefore, the energy stored in the leakage inductor must discharge $C_{DS,M1}$ to the voltage level of 0 V before switch $M_1$ is turned on. The energy required to discharge the charge of the metal–oxide–semiconductor field-effect
Fig. 7. Theoretical voltage conversion ratio according to the switching frequency.

Fig. 8. Required dead time for the ZVS of the proposed converter.

transistor’s (MOSFET) nonlinear output capacitance can be derived from datasheet parameters. Assuming that the capacitance is an inverse square-root function of its voltage, we can use energy equivalence relationships to express the stored energy in terms of a small-signal measurement [20]. The energy required to achieve the ZVS is given as

\[ E_{\text{required}} = \frac{8}{3} C_{\text{oss}} \sqrt{V_{\text{oss}} V_{\text{in,max}}^3} \]  

where \( C_{\text{oss}} \) is a small-signal MOSFET’s equivalent output capacitance measured at the drain–source voltage \( V_{\text{oss}} \). The energy stored in the leakage inductance is given as

\[ E_{\text{stored}} = \frac{1}{2} L_k I^2 = \frac{1}{2} L_k \left( I_V + \frac{\text{PL} \times I_o}{n} \right)^2 \]  

where PL is defined as the ratio between the minimum load current for ensuring the ZVS and the maximum load current. To ensure the ZVS, the energy \( E_{\text{stored}} \) stored in the leakage inductance \( L_k \) must be greater than the energy \( E_{\text{required}} \) stored in the switch output capacitor. Therefore, the required minimum leakage inductance can be determined from (21) and (22) as

\[ L_{k, \text{min}} \geq \frac{16 C_{\text{oss}} \sqrt{V_{\text{oss}} V_{\text{in,max}}^3}}{3 \left( I_V + \frac{\text{PL} \times I_o}{n} \right)} \]  

The required dead time (see Fig. 8) to achieve the ZVS is given as

\[ t_{\text{dead}} = \frac{2 C_{\text{oss}} (V_{\text{in}} + V_V)}{I_V + \left( \frac{I_v}{n} \right)} + \pi \sqrt{L_k C_{\text{oss}}} \]  

where \( f_{\text{eff}} \) is the effective switching frequency. It is shown in (28) that the larger leakage inductance \( L_k \) produces the larger duty cycle loss and the higher effective switching frequency.

\[ \Delta T = L_k \left( \frac{2 I_v}{n} \right) \approx 2 L_k I_o \quad (26) \]

\[ f_{\text{eff}} = \frac{1}{T_s - 2 \Delta T} \quad (27) \]

\[ \Delta D = \frac{\Delta T}{T_s} \quad (25) \]

\[ \Delta I_o = \frac{\left[ \left( C (V_V + V_{\text{in}}) I_V - \frac{L_k}{n} \right) \right.}{\left. \frac{L_k}{n} \left( I_V - \frac{L_k}{n} \right)^2 + (V_V + V_{\text{in}})^2 \right]} \]  

\[ L_{o, \text{ZVS PSFB}} = \left[ \frac{V_{\text{in}}}{n_{\text{ZVS PSFB}}} - V_o \right] \Delta I_o \quad (28) \]

\[ L_{o, \text{proposed}} = \left[ \frac{V_{\text{in}} - v_{C}(t)}{n} - V_o \right] \Delta I_o \quad (29) \]

IV. DESIGN EXAMPLE

To verify the feasibility of the proposed converter, a simple design example with the following specifications is taken.

A. Design Specifications

1) Input voltage \( V_{\text{in}} \): 320 - 400 V;
2) Output voltage \( V_o \): 12 V;
3) Output power $P_o$: 1200 W;
4) Switching frequency $f_{sw}(V_{in} = 400 \text{ V}, I_o = 100 \text{ A}) = 60 \text{ kHz}.$

**B. Transformer Turn Ratio**

As mentioned in Section III, the turn ratio of transformer can be decided from (20). In addition, to ensure the regulated output voltage, the transformer turn ratio $n$ must be decided at the minimum input voltage. When the input voltage is minimum (320 V), the converter is operated at the minimum switching frequency $f_{sw, \text{min}}/f_o$. If $f_{sw, \text{min}}/f_o$, which is the designer’s choice and is proportional to the switching frequency variation, is chosen as 1.9, the transformer turn ratio $n$ can be calculated as 35.

**C. Magnetizing Inductor $L_m$ and Boost Capacitor $C_r$**

$f_{sw, \text{max}}/f_o$ can be calculated as 4.1 from (20) when the input voltage is maximum (400 V). Assuming that the switching frequency at the maximum input voltage (400 V) is chosen as 60 kHz, considering the overall system efficiency and volume, the minimum switching frequency at the minimum input voltage (320 V) can be obtained as 27.8 kHz from (20). In particular, if the voltage across the boost capacitor exceeds $(V_{in} + V_o)$, the proposed converter cannot properly operate, where $V_o$ is the increased amount in $\Delta v_C$, by the energy stored in the leakage inductor after $v_C(t)$ becomes equal to $V_{in}$. Assuming that the leakage inductance $L_k$ is 2% of the magnetizing inductance $L_m$, the characteristic impedance $Z$ should be designed to be less than 136.7 from (31). Finally, the magnetizing inductance $L_m$ and the boost capacitor $C_r$ are calculated as follows:

\[
V_a = \sqrt{\frac{L_k}{C_r}} \left( I_v + \frac{I_o}{n} \right) \approx \frac{1}{10} \sqrt{\frac{2L_m}{C_r}} \left( I_v + \frac{I_o}{n} \right) 
\]

\[
Z \leq \frac{V_{in, \text{min}}}{I_v} + \sqrt{\frac{3}{10}} \frac{V_{in, \text{min}} \sin(0.5\omega_{sw}/f_{sw, \text{min}})}{n(1 + \cos(0.5\omega_{sw}/f_{sw, \text{min}}))} 
\]

\[
= 136.7 \text{ [\Omega]} 
\]

\[
L_m \leq \frac{Z}{\omega_o} = 1487.2 \text{ [\mu H]}, 
\]

selected as $L_m = 1000 \text{ [\mu H]}$

\[
C_r \geq \frac{L_m}{Z^2} = 53.5 \text{ [nF]}, \text{ selected as } C_r = 66 \text{ [nF]}. 
\]

**V. SIMULATION AND EXPERIMENTAL RESULTS**

In order to verify the operation of the proposed converter, PSIM simulation and experiment are performed with the specifications of the input voltage $V_{in} = 320\text{—}400 \text{ V}$, the output voltage $V_o = 12 \text{ V}$, the maximum output power $P_o, \text{max} = 1.2 \text{ kW}$, the holdup time $t_o = 20 \text{ ms}$, the magnetizing inductor $L_m = 1 \text{ mH}$, the leakage inductor $L_k = 22 \text{ \mu H}$, the output inductor $L_o = 1.8 \text{ \mu H}$, the boost capacitor $C_r = 66 \text{ nF}$, and the output capacitor $C_o = 1550 \text{ \mu F}$.

**A. Simulation Results**

Fig. 9 shows the simulation results of the conventional ZVS PSFB and proposed PFB-SBC full-bridge converters. To compare the proposed converter with the conventional ZVS PSFB converter, simulations are performed under the same conditions such as the switching frequency $f_{sw}$, the magnetizing inductance $L_m$, and the output inductor $L_o$. As a result, the conventional ZVS PSFB converter has long freewheeling intervals of about 0.27$\tau_s$, and thereby, the peak primary current $I_{pri, \text{max}}$ is measured as 7.18 A. On the other hand, the peak primary current $I_{pri, \text{max}}$ of the proposed converter is measured as 4.62 A, which is because there exist no freewheeling intervals in the proposed converter. Moreover, while the output inductor current ripple $\Delta i_{Lo,\text{PFM SBC}}$ of the proposed converter is as small as 8.48 A, $\Delta i_{Lo,\text{ZVS PSFB}}$ of the conventional converter is 25 A under the same output inductor $L_o = 1.8 \text{ \mu H}$. Therefore, the output inductor of the proposed converter and the subsequent conduction loss can be more reduced than those of the conventional ZVS PSFB converter.

**B. Experimental Results**

The prototype of the proposed converter shown in Fig. 2 is implemented with the specifications of primary switches $M_1 - M_4 = \text{SPP20N60C3}$, transformer core = two overlapped EI3329 (volume : 15280 mm$^3$, $\mu_r : 2070$), transformer turn ratio = 35:1:1, output inductor core = CH270060 (volume : 4154 mm$^3$, $\mu_r : 60$), boost capacitor $C_r$ = polypropylene film capacitor of 33 nF(2EA), and synchronous rectifiers (SRs) $M_{SR1}/M_{SR2} = \text{IRFB3070}$. To reduce the transformer copper losses caused by the proximity effect, a sandwich winding method is employed, which can reduce the alternating-current resistance depending on the wire type, mean length, and
operating frequency. Moreover, to reduce the conduction losses of the output rectifier, the SRs are employed in the transformer secondary side.

Fig. 10 shows the key waveforms of the $M_1$ gate signal, the drain–source voltage $V_{ds,M1}$ across switch $M_1$, and the transformer primary current $i_{pri}$. Moreover, Table I shows the measured data of the proposed converter. Although the small difference between the measured and calculated output voltages exists, they well coincide with the aforementioned theoretical results. This small difference originated from the duty cycle loss, as stated above. Since switch $M_1$ is turned on after the drain–source voltage drops to 0 V, the ZVS can be achieved. Moreover, since the switching frequency variation is not so wide as to the range of 58.8 ($I_o = 100$ A) to 76.8 kHz ($I_o = 0$ A), the reactive components such as the inductor, the transformer, and the capacitors can be easily designed to be operated at optimum conditions. As shown in this figure, the primary dc offset current and the freewheeling intervals do not exist with the aid of the 50% fixed duty operation. Thus, it cannot only reduce the size of the transformer but also improve the device heat generations and system efficiency. As shown in Fig. 10(d), the peak and RMS values of the primary current measured at full load condition are not so large, i.e., 4.3 and 3.557 A, respectively.

When the output inductor $L_o$ is 1.8 $\mu$H, Fig. 11(a) shows the current ripple through the output inductor at the full-load condition. While the current ripple of the conventional ZVS PSFB converter is 25 A, that of the proposed converter is as small as 12.9 A with $L_o = 1$. In addition, when the output inductor is reduced from 1.8 to 1 $\mu$H, Fig. 11(b) shows that the current ripple through the output inductor is 17.1 A. Although the current ripple is increased by 4.2 A, it is still smaller than that of the ZVS PSFB converter. Therefore, the reduced wire length can considerably reduce the copper loss of the inductor wire. Moreover, the size of the output capacitor can be also reduced due to the reduced RMS current through the capacitor.

Fig. 12 shows the comparison of the measured efficiency between the conventional ZVS PSFB and proposed converters. As shown in this figure, the proposed converter can achieve approximately 2% higher efficiency along wide load ranges (20–100 A), and its efficiency at the full-load condition is as high as 96.57%. This high efficiency originated from no freewheeling interval, reduced ripple current through the output inductor, and subsequent reduced conduction losses with the aid of the 50% fixed duty operation.

### TABLE I

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*Test equipment: YOKOGAWA WT1600 DIGITAL POWER METER
Electronic load EML-130L
Dual display Multimeter

VI. CONCLUSION

The PFM-SBC full-bridge dc/dc converter has been proposed in this paper. The conventional ZVS PSFB converter has large circulating energy during the freewheeling interval caused by the small duty cycle, which could increase the primary-side
proposed converter, experimental results from a prototype of to confirm the operation, the features, and the validity of the inductor, high efficiency, and improved heat generation. Finally, Therefore, it has very desirable merits such as small output all power switches can be achieved along wide load ranges. conduction losses, the turn-off switching losses of lagging-leg switches, and the current ripple through the output inductor. To overcome these problems, the proposed converter regulates the output voltage by varying the voltage across the SBC according to the switching frequency and has no freewheeling interval with the aid of the 50% fixed duty operation. As a result, it can considerably reduce conduction losses and current ripple through the output inductor, as compared with the conventional ZVS PSFB converter. Moreover, the ZVS operation of all power switches can be achieved along wide load ranges. Therefore, it has very desirable merits such as small output inductor, high efficiency, and improved heat generation. Finally, to confirm the operation, the features, and the validity of the proposed converter, experimental results from a prototype of 400–12 V/100 A have been presented. The experimental results have verified the validity of the operational principle and have demonstrated that the proposed converter can achieve efficiency as high as over 96.25% along load ranges of 20–100 A. The proposed converter having these favorable advantages is expected to be well suited for high-power-density applications.

REFERENCES


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